IN THE SPECIFICATION

Replace the paragraph beginning on page 1, lines 30 and 31, with the following:

FIG.1 is a top plan view showing a ~~portion~~ portion of a cell area of a general NAND type flash memory.

Replace the paragraph beginning on page 2, lines 21 to 34, and continuing on page 3, lines 1 to 6, with the following:

In a process of forming a cell area of a flash memory device shown in FIG.1 to FIG.3, first an isolation insulating layer 23 is formed on a substrate 20 to define an active region by means of a general shallow trench isolation (STI) process. The active region comprises a plurality of line shaped sub-regions. Thereafter, a gate insulating layer 24 is formed in the active region. Then, a plurality of gate lines comprising string select gate lines 33s, a plurality of word lines WP, and ground select gate lines 33g are formed to cross the active region. Also, source/drain regions 35', are formed to be overlapped with a plurality of line shaped sub-regions of the active region by doping an impurity on the exposed surface of the substrate between the gate lines. The source/drain regions 35', formed by general ion implantation processes of using the gate lines and spacer 37 on both side walls of the gate lines as a mask, form a dual doped structure. Namely, highly doped portions are formed in the active region of the substrate between the adjacent spacers 37, and lightly doped portions in the active region of the substrate between the gate lines and the highly doped portions, i.e., in the active region of the substrate under the spacers 37. Then, an interlayer insulating layer 41 is deposited and planarized. Thereafter, a groove is formed to expose the common source regions 35s' between the ground select gate lines 33g and filled with a conductor such as a polysilicon layer to form a common source line 45. Then, after an interlayer insulating layer 49 is formed over the resultant substrate, contact holes are formed to expose drain regions 35d' of the string select gate lines 33s, and are then filled with a conductive layer to form bit line contacts. And then, bit lines are formed.

Replace the paragraph beginning on page 3, lines 31 to 33, with the following:

It is ~~other~~ another object of the present invention to provide an improved semiconductor device and method of manufacturing the same, in which a metal silicide layer is not formed in source/drain regions, but on gate lines.

Replace the paragraph beginning on page 4, lines 1 to 4, with the following:

It is ~~ether~~ another object of the present invention to provide an improved semiconductor device and method of manufacturing the same, which can prevent break down in channels and current leakage of source/drain regions from occurring , when width of the gate line having a metal silicide layer is below 0.15μm.

Replace the paragraph beginning on page 4, lines 11 to 14, with the following:

In the semiconductor device of the invention, the semiconductor layer is formed of a silicon substrate. Also, the impurity implantation is carried out by a dose of impurity below 1.0×10^{15} ions/ cm^2 to prevent break down from occurring in channels of the device, for example the device in which the width of the gate line is below 0.15μm.

Replace the paragraph beginning on page 8, lines 19 to 30, with the following:

Referring to FIG.7, after the ion implantation, a plurality of insulating spacers 137, each being composed of a nitride layer or an oxide layer, are formed on side walls of the gate electrodes 133. The spacers 137 are formed by using a method of depositing an insulating layer over the substrate 120 over which the gate electrodes 133 are formed, and etching anisotropically the whole surface of the substrate 120 over which the insulating layer are formed. After forming the spacers 137, a relatively high concentration impurity implantation is carried out by using the gate lines and the spacers 137 as a mask. At this time, an impurity concentration is restrained to prevent break down in transistor channels under the gate lines from being occurred. Thus, source/drain regions 135' having dual doped structures are formed and a MOS transistor structure is obtained. For a ~~sequent~~ subsequent process, an etch stop layer 139 is formed of a silicon nitride layer having a thickness of 1,000Å over the whole surface of the substrate 120.